REMARKS

Applicant submits the above amendments and following remarks in response to the final Office Action of the parent application, Application Serial No. 09/410,328, which was mailed on 10 April 2001.

Specifications:

The specification has been amended to correct minor informalities. No new matter has been added.

Claims:

The above amendments amend the claims to recite more definitely the claimed subject matter. No new matter has been added. By the present amendment, claim 12 has been amended and new claims 21-33 have been added. Claims 12 and 21-33 are pending in the application. Amendment to the claims should in no way be construed to be an acquiescence to any of the rejections. Amendment to the claims are being made solely to expedite the prosecution of the above-identified application. Applicant reserves the option to further prosecute the same or similar claims in the instant or subsequent patent applications.

Response to the final Office Action dated September 11, 2001:

The issues raised in the parent application's final Office Action are addressed below in the order in which they were presented in the Office Action:

1. Claim Objections

The final Office Action objected to claims 13, 16-24, 26-28 and 30-31 of the parent application due to claim informalities. The objections raised in the Office Action have been addressed in the new claims presented herein.

2. Rejection of Claims Under 35 U.S.C.§112

The final Office Action rejected claims 13 of the parent application under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the

specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The Office Action stated that the phase "decoupling capacitor connects in parallel between said power and ground planes" of claim 13 is not described in the specification or shown in the figures. New claim 22 includes language which is identical to the language of the patent application's claim 13. The first full paragraph of the specification found on page 9 has been amended to describe the elements found in claim 22 (of the present application). Claim 13 of the parent application was included in the parent application as originally filed. Based upon the specification and claim 13, as both were originally filed in the parent application, persons skilled in the art would reasonably conclude that the Applicants were in possession of the invention claimed in claim 13 (now claim 22).

The final Office Action rejected claims 20, 23, 25, 26, 28 and 31 of the parent application under 35 U.S.C. § 112, second paragraph, as being indefinite. The rejections raised in the Office Action have been addressed in the new claims presented herein or are now moot.

3. Rejection of Claims Under 35 U.S.C.§102(b)

The final Office Action rejected claims 12, 13, 16-20, 23-26 and 28-31 of the parent application under 35 U.S.C. § 102(b) as being anticipated by Tuckerman [U.S. Patent 5,274,270]. Amended independent claim 12 of the present application recites a device for interconnecting a plurality of circuit devices where the device includes a support base having a first surface, a decoupling capacitor mounted on the first surface and an interconnect layer having a pattern of circuit connections and being formed over the decoupling capacitor and embedded within the interconnect layer and whereby the pattern of circuit connections of the interconnect layer is coupled to the decoupling capacitor and a plurality of circuit devices mounted on a surface of the interconnect layer opposite the first surface of the support base.

Tuckerman fails to disclose or teach the limitations of Applicants' amended claim 12. At a minimum, Tuckerman fails to disclose or teach a device having a pattern of

circuit connections of an interconnect layer *coupled to a decoupling capacitor and a plurality of circuit devices* which are mounted on a surface of the interconnect layer opposite the first surface of the support base. The circuit connections 76, 77 of Tuckerman are not coupled to the decoupling capacitor 49, as is recited in Applicants' claim 12. See Fig. 3. Moreover, the circuit connections 76, 77 of Tuckerman are not coupled to the circuit device 90. Instead, Tuckerman utilizes a lead 98 to electrically connect the circuit connections 76, 77 to the circuit device 90. Accordingly, Tuckerman does not disclose nor teach all the limitations of Applicants' claim 12.

The final Office Action rejected claims 12, 13 and 17-20 of the parent application under 35 U.S.C. § 102(b) as being anticipated by Eichelberger [U.S. patent 5,841,193]. At a minimum, Eichelberger fails to disclose or teach a device having a support base and a pattern of circuit connections of an interconnect layer coupled to a plurality of circuit devices *which are mounted on a surface of the interconnect layer opposite the first surface of the support base*, as is recited in Applicants' claim 12. The plurality of circuit devices 12, 102 found in Eichelberger are mounted *on* the support base 14, 120 and not on a surface of an interconnect layer opposite the first surface of the support base. See Figs. 1-5 and col.1, line 66-67 *("Structures in accordance with the present invention fall into the category of chips first MCMs.")*. Accordingly, Eichelberger does not disclose nor teach all the limitations of Applicants' claim 12.

4. Rejection of Claims Under 35 U.S.C.§102(e)

The final Office Action rejected claims 12, 13, 16-20, 25-26 and 29-31 of the parent application under 35 U.S.C. § 102(e) as being anticipated by Gardner [U.S. Patent 5,973,910]. At a minimum, Gardner fails to disclose or teach a device that has an a decoupling capacitor mounted on the first surface and an interconnect layer having a pattern of circuit connections and being formed over the decoupling capacitor whereby the pattern of circuit connections of the interconnect layer is coupled to the decoupling capacitor *and a plurality of circuit devices mounted on a surface of the interconnect layer opposite the first surface of the support base*, as is recited in Applicants' claim 12. Gardner does not disclose nor teach a having a plurality of circuit devices mounted on a

surface of the interconnect layer opposite the first surface of the support base. See Figs 1-8. On the contrary, Gardner specifically states that the Gardner capacitor is typically formed on a substrate (i.e., a support base) having *underlying* circuitry or device layers. See col. 2, lines 57-58. Accordingly, Gardner does not disclose nor teach all the limitations of Applicants' claim 12.

Thus, based on the prior art cited by the Examiner, Applicants accordingly assert that claim 12 is allowable. Claims 21-33 depend upon claim 12.

Conclusion

By the present Preliminary Amendment, claim 12 has been amended and new claims 21-33 have been added. Claims 12 and 21-33 are pending in this application. Attached hereto is a marked-up version of the changes made to the specification and claims be the present Preliminary Amendment. The attached page is captioned "Version with markings to show changes made."

Based on the above Amendment and Remarks, Applicants respectfully submits that pending claims 12 and 21-33 are in condition for allowance and favorable consideration and allowance are earnestly solicited.

Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-832-1000 (direct dial: 617-832-1716).

Respectfully submitted,
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Version with markings to show changes made:

In the Specification:

Paragraph beginning at line 8 of page 9 has been amended as follows:

Turning to Figure 2, one portion, section A, of the MCM module 10 depicted in Figure 1 is shown in greater detail. Specifically, Figure 2 presents an enlarged view of section A of the MCM module 10, and more specifically depicts the support base 12 having disposed thereon the decoupling capacitor 14 which is embedded within the interconnect layer 16. Figure 2 presents a cross-sectional view of this portion of the MCM device 10 which cross-sectional view illustrates that the MCM device 10 is a multilayer device. Figure 2 further shows that the decoupling capacitors 14 can be electrically coupled to the ground plane 29 and power plane 28 [for] of the MCM module 10. In certain exemplary embodiments, the decoupling capacitor 14 may be connected in parallel with the power plane 28 and the ground plane 29. Figure 2 further depicts that the interconnect layer 16 can include a plurality of layers that can be organized into a pattern of circuit connections that can be employed for interconnecting the circuit devices 20 mounted to the surface 18 of the interconnect layer 16. Figure 2 further shows that the interconnect layer 16 can include power and ground connections, 31 and 33, that can provide power to the circuit devices 20 and which are decoupled by the decoupling capacitors 14.

Paragraph beginning at line 18 of page 10 has been amended as follows:

Figures 3A - 3B depict one particular embodiment of a decoupling capacitor 30 that can be employed with the MCM 10 depicted in Figure 1. The depicted decoupling capacitor 30 is a component that is mounted to the support base 12 before the interconnect layer 16 is formed. The decoupling capacitor 30 can comprise a thin film MCM-D technology fabricated device, and in particular can be formed by multi-layer thin film processing with copper or aluminum metallization and SiO_2 dielectric material fabricated on a silicon based substrate. One such capacitor and techniques for forming such a capacitor is generally described in the above referenced U.S. Patent 5,134,539.

Paragraph beginning at line 27 of page 10 has been amended as follows:

Figure 3A provides a overhead view of the decoupling capacitor device 30 that is formed as a component level device and which is capable of decoupling a power plane and a ground plane for an MCM device. The decoupling capacitor 30 is a silicon base die decoupling capacitor with an embedded ground and power plane and a SiO_2 dielectric material disposed therebetween. The decoupling capacitor 30 can be sized and shaped for the application at hand, and the depicted decoupling capacitor 30 is not to be understood as an exhaustive representation of the structure of the decoupling capacitors suitable for use with the present invention. Moreover, other dielectric materials can be employed, and the type of dielectric will depend upon the application. It is understood however that the silicon material dielectric should [is] provide[s] good thermal expansion properties. As shown in Figure 3A the depicted decoupling capacitor 30 includes a first section 32 and a second section 34. Thus a given die can support more than one capacitor. The first section 32 of the depicted decoupling capacitor 30 comprises six individual capacitors each of which share a common ground plane. In this depicted embodiment, each of the six individual capacitors 36 are substantially the same size, thereby providing substantially the same capacitance. The second portion 34 of the depicted capacitor 30 comprises two capacitors 44 each of approximately the same size, and each larger than the individual capacitors 36 of the first portion 32. Accordingly, it will be understood that the individual capacitors 44 provide greater capacitance than the individual capacitors 36 of the first portion 32. The size and the shape of the capacitors can vary depending upon the application, and those of ordinary skill in the art will be able to select the proper capacitance for decoupling the circuit. Further, the distribution, arrangement of the capacitors can vary depending upon the application, and for example, separate capacitors, with separate ground planes can be employed for decoupling different circuit devices to for example allow separate decoupling of analog and digital circuit devices. These arrangements can vary depending upon the application.

Paragraph beginning at line 24 of page 11 has been amended as follows:

For both capacitors 36 and 44 [34], the top surface comprises a plurality of pads each of which can be employed for forming an electrical connection with the interconnect layer 16 that can be formed over these decoupling capacitors. Turning to Figure 3B a cross-sectional view is presented of these decoupling capacitors 36 and 44. Specifically, Figure 3B shows a silicon base 48 upon which a ground plane 50 is disposed. Above the ground plane is a power plane 52. Disposed between the power plane 52 and the ground plane 50 is a dielectric material which can be any suitable dielectric material such as SiO_2, polyimide or any other suitable material. The ground planes 50 and power planes 52 can be formed of aluminum, copper, aluminum oxide or other conductive material. The power planes, ground planes and dielectric material can be stacked in layers to provide a selected capacitance appropriate for the application. As further shown by Figure 3B, gaps 54 can be disposed at locations within the power or ground planes that allow for separating the power and ground planes from each other thereby preventing a short circuit. The metal layers within the interconnect layer 16 can electrically couple to these pads, thereby connecting the circuit pattern to the power and ground planes at a location that is proximate to, or at, the location of the decoupling capacitors. This allows for minimizing the interconnect distance.

Paragraph beginning at line 28 of page 13 has been amended as follows:

Figure 6 depicts that an interconnect layer 16 can be formed on top of the component layer. In one practice, an *in situ* process can be performed wherein a dielectric layer is directly deposited on the upper surface of the plurality of components, in this case the decoupling capacitors 14 and the resistive element 22. Further processing can include patterning and forming vias in the *in situ* formed dielectric layer. The vias can be disposed within this layer to expose at least some of the contact pads at the upper surface of the decoupling capacitors 14 and the resistive element 12. Such exposed contacts facilitate electrical connections to the connecting layers that can be later deposited. To this end, the forming of a metalization structure above the *in situ* processed dielectric can occur in a manner that allows metalization within the vias. Metal formed within the vias can create electrical connections to at least some of the contact pads exposed by the vias and carried on the surface of the components. For the

interconnect layer 16 depicted in Figure 6, a plurality of layers have been deposited in sequence to form the circuit pattern. Accordingly, in subsequent steps further chip interconnect layers can be added by alternatively applying dielectric and metalization layers. Although photo patterning of the deposited dielectric layers provides one process for forming the interconnect layer 16, it will be understood by those of ordinary skill in the art that other techniques can be employed for depositing the interconnect layer and thereby forming the circuit pattern for the MCM device. Moreover, it will be understood by those with ordinary skill in the art that although the interconnect layer 16 depicted in Figure 6 is shown as having a plurality of metalized layers, that such a module can be formed with a single layer, or two layers, and that no specific number of layers is necessary for the practice of the invention. Additionally, it will be understood that in optional embodiments and practices, decoupling capacitors and other components, can be disposed between metallic layers, by placing these devices on the interconnect layer partially through the deposition process.

In the Claims:

12. (Amended) A device for interconnecting a plurality of circuit devices, comprising:

a support base having a first surface[,];

a decoupling capacitor mounted on said first surface[,]; and

an interconnect layer having a pattern of circuit connections and being formed over [and surrounding] said decoupling capacitor, whereby said decoupling capacitor is embedded within said interconnect layer,

and whereby said pattern of circuit connections of said interconnect layer is coupled to said decoupling capacitor and a plurality of circuit devices mounted on a surface of said interconnect layer opposite said first surface of said support base.